WHAT IS CLAIMED IS:

1. A process for fabricating a semiconductor device, comprising:

providing a semiconductor substrate of a first conductivity;

epitaxially growing an undoped intrinsic semiconductor body over a major surface of said semiconductor substrate;

implanting dopants of a second conductivity into said intrinsic semiconductor body to a first depth;

implanting dopants of said first conductivity into said intrinsic semiconductor body to a second depth, said second depth being farther from a free surface of said semiconductor body than said first depth and closer to said substrate than said first depth; and

applying heat to said semiconductor body to at least activate said dopants of said first conductivity and said dopants of said second conductivity and to diffuse said dopants until said dopants of said first conductivity and said dopants of said second conductivity meet inside said semiconductor body; whereby a channel region is formed over a drift region in said semiconductor body.

2. A process according to claim 1, further comprising forming a gate structure adjacent said channel region, said gate structure comprising a gate insulation layer adjacent said channel region, and a gate electrode adjacent said gate insulation layer.

3. A process according to claim 2, wherein said gate insulation layer is comprised of silicon dioxide and said gate electrode is comprised of polysilicon.

4. A process according to claim 2, further comprising forming a trench in said semiconductor body extending through said channel region into said drift region, and disposing said gate structure in said trench.

5. A process according to claim 4, further comprising forming a conductive region of said first conductivity adjacent said gate structure in said semiconductor body, said conductive region extending to a third depth, said third depth being closer to said free surface of said semiconductor body than said first depth.

6. A process according to claim 5, wherein said conductive region is a source region and said semiconductor substrate serves as the drain region.

7. A process according to claim 6, further comprising creating a recess in said semiconductor body, said recess extending to a depth below that of said source region and exposing said channel region, and further comprising forming a source contact over said free surface of said semiconductor body in electrical contact with said source region and said channel region.

8. A process according to claim 7, wherein said recess includes tapered sidewalls.

9. A process according to claim 7, wherein said recess includes vertical sidewalls.

10. A process according to claim 7, further comprising implanting dopants of said second conductivity at the bottom of said recess prior to forming said source contact.

11. A process for fabricating a semiconductor die, comprising:

providing a semiconductor wafer of first conductivity;

epitaxially growing an undoped intrinsic semiconductor body over one major surface of said semiconductor wafer, said semiconductor body having a free surface opposite said semiconductor wafer;

forming a region of second conductivity in said semiconductor body at a first depth below said one major surface;

forming a region of said first conductivity in said semiconductor body at a second depth below said first depth;

applying heat to said semiconductor body to activate said dopants of said first and second conductivity, and to diffuse said dopants until said region of said second conductivity reaches said region of said first conductivity, whereby a channel region is formed from said region of said second conductivity and a drift region is formed from said region of said first conductivity;

forming a plurality of identical devices in said semiconductor body, each one of said identical devices constituting a die; and

singulating each die.

12. A process according to claim 11, further comprising forming a gate structure adjacent said channel region in each said die, said gate structure comprising a gate insulation layer adjacent said channel region, and a gate electrode adjacent said gate insulation layer.

13. A process according to claim 12, wherein said gate insulation layer is comprised of silicon dioxide and said gate electrode is comprised of polysilicon.

14. A process according to claim 12, further comprising forming a trench in said semiconductor body extending through said channel region into said drift region, and disposing said gate structure in said trench in each said die.

15. A process according to claim 14, further comprising forming a conductive region of said first conductivity adjacent said gate structure in said semiconductor body in each said die, said conductive region.

16. A process according to claim 15, wherein said conductive region is a source region.

17. A process according to claim 16, further comprising creating a recess in said semiconductor body, said recess extending to a depth below that of said source region and exposing said channel region, and further comprising forming a source contact over said free surface of said semiconductor body in electrical contact with said source region and said channel region in each said die.

18. A process according to claim 17, wherein said recess includes tapered sidewalls.

19. A process according to claim 17, wherein said recess includes vertical sidewalls.

20. A process according to claim 17, further comprising implanting dopants of said second conductivity at the bottom of said recess prior to forming said source contact in each said die.

21. A process for fabricating a semiconductor wafer, comprising:

providing a semiconductor substrate of first conductivity;

epitaxially forming an undoped intrinsic semiconductor body over a first major surface of said substrate;

implanting dopants of second conductivity into said semiconductor body to a depth below a free surface of said semiconductor body;

implanting dopants of said first conductivity into said semiconductor body to a depth below said depth of said dopants of said second conductivity; and

applying heat to said semiconductor body for a period of time at a selected temperature to activate said dopants and to diffuse the same until at least said dopants of said first conductivity reach said dopants of said second conductivity,

whereby said dopants of said first conductivity form a drift region coextensive with a channel region along the lateral direction in said semiconductor body.

22. A process according to claim 21, wherein said substrate has a diameter that is larger than six inches.

23. A process according to claim 21, wherein the thickness of said epitaxial body, said depth of said dopants of said first conductivity, said depth of said dopants of said second conductivity, said period of time and said temperature are selected so that said drift region reaches at least said semiconductor substrate.

24. A process according to claim 21, wherein the thickness of said epitaxial body, said depth of said dopants of said first conductivity, said depth of said dopants of said second conductivity, said period of time and said temperature are selected so that said channel region reaches said free surface of said semiconductor body.